IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Kevin M. Christiansen
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TITLE:	System for Data Transfer Through an I/O Device Using A Memory Access Controller Which Receives and Stores Indication of a Data Status Signal
EXAMINER:	Eron J. Sorrell
GROUP ART UNIT:	2182
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Dated: March 18, 2008

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APPEAL BRIEF

Real Party in Interest

The subject application is owned by Apple Inc. of Cupertino, California.

Related Appeals and Interferences

There are no known related appeals or interferences that may directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

Status of Claims

Claims 1-20 stand allowed. Claims 21-36 stand finally rejected. On January 18, 2008, Appellant appealed from the final rejection of claims 21-36. The claims on appeal are set forth in an appendix attached hereto.

Status of Amendments

Appellant has not amended the claims since the final rejection.

Summary of Claimed Subject Matter

The independent claims on appeal are claims 21, 26, 30 and 34. Claims 21, 26 and 30 comprise a memory access controller for transferring a data unit from a computer system memory to a system or device external to the computer system (e.g., FIGS. 1, 5, 6; Spec. col. 1, line 64 to col. 2, line 14; col. 5, lines 3-25). A memory, such as channel status register 110 or status register 250, stores a data status signal generated by an I/O device 20, such as an Ethernet controller 140. (e.g., FIGS. 1, 4; Spec., col. 3, lines 45-57 and 58-60, col. 5, lines 19-29). The data status signal is generated by the I/O device after transferring a data unit to a system external to the computer system, such as external device system 50 (e.g., FIG. 1; Spec., col. 3, lines 45-57, col. 5, lines 3-25). Circuitry, such as bus interface 70 or DMA engine 60, is coupled to the memory, such as status register 250 or channel status register 110, and controls subsequent operation of the memory access controller based on the status data.

Similarly, claim 34 comprises a method for transferring a data unit between a memory with a computer system and a memory external to the computer system using memory access controller 10 coupled to the memory 90 and an Input/Output device 20 (e.g. FIGS. 1, 5; Spec.,

col. 3, lines 45-57, col. 5, lines 3-19). Status data, generated by the Input/Output device 20, is used to indicate completion of the data unit transfer (FIG. 5, Spec., col. 5, lines 15-28). The status data is stored in memory and used to control subsequent operation of the memory access controller 10 (Spec. col. 5, lines 23-35).

As required by 37 CFR 41.37(c)(v), it is noted that independent claim 26 recites means plus function elements as permitted by 35 U.S.C. § 112, sixth paragraph. Examples of a structure corresponding to the means for storing a data status signal are the channel status register 110 and the status register 250 (e.g., FIGS. 1, 4; Spec., col. 3, lines 58-60, col. 5, lines 19-29). Examples of a structure corresponding to the means for controlling subsequent operation of the memory access controller using the data status signal are the channel control register 110 and the status register 250 (e.g., Spec. col. 3, lines 57-67, col. 5, lines 19-41).

Grounds of Rejection to be Reviewed on Appeal

Whether claims 21-36 are unpatentable under 35 U.S.C. § 103(a) over U.S. Patent No. 5,584,010 to Kawai et al. ("Kawai") and U.S. Patent No. 5,614,685 to Matsumoto et al. ("Matsumoto").

Argument

To establish a *prima facie* case of obviousness, the cited references, when combined, must teach or suggest all the claimed elements. *In re Royka*, 490 F.2d 981 (CCPA 1974); *see also In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988) (reversing § 103 rejection because examiner ignored material claimed limitation that was absent from reference). As the suggested

combination of references fails to teach or suggest all of the limitations of the rejection claims, the Examiner's obviousness rejection was improper.

Specifically, the suggested combination of Kawai and Matsumoto fails to disclose or suggest "a register that stores a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer," "means for storing a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer system," or "a memory configured to store status data generated by an Input/Output (I/O) device after a data unit transfer between the computer system memory and a system external to the computer system" as variously recited in the independent claims

Representative claim 21 recites a memory access controller adapted to be coupled to a computer system memory and an Input/Output (I/O) device comprising:

> a register that stores a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer; and
>
> circuitry coupled to the register that receives the data status signal and for controlling subsequent operation of the memory access controller based on the data status signal.

Hence, the data status signal indicates when the I/O device has transferred a data unit to a system external to the computer, allowing operation of the memory controller to be controlled without requiring information from the computer system's host processor. This beneficially reduces the time needed to transfer data to a system external to the computer.

As the Examiner admits in the Final Office Action dated September 18, 2007, Kawai fails to disclose a register or other storage device which "stores a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer," as claimed. *See* Final Office Action dated September 18, 2008, ¶ 4, page 3. Instead, Kawai

discloses a multi-processor system having multiple digital signal processors (DSPs). Each DSP has an internal, i.e., "on-chip," memory, but the multi-processor system also includes an "external data memory" i.e., "off-chip memory,", which is accessed by the DSPs through a main data bus (Kawai, FIG. 5; col. 6, lines 65 to col. 7, line 24). The only data transfers disclosed in Kawai are transfers of data between the DSP and this off-chip memory. As used in Kawai, "external" merely refers to off-chip as opposed to on-chip memory.

Matsumoto does not remedy the deficient disclosure of Kawai. Matsumoto merely discloses a musical tone signal processing device including a central processing unit (CPU), a DSP and a memory (Matsumoto, col. 3, lines 2-10). The DSP includes a data I/O control portion for performing a data input/output control on data transmitted between the DSP and an "external device or system" (Matsumoto, col. 3, lines 60-67). However, Matsumoto only uses the term "external device or system" once in the specification and provides no further description of this term. There is no clarification in Matsumoto of whether the referenced "external device or system" is external to the system including the DSP or is merely external to the DSP itself. The mere reference in Matsumoto to an "external device or system" without clarification of how the term "external" is used does not disclose "," as specifically claimed.

Matsumoto does describe an "external data memory," which is separate from the DSP but included in the same system as the DSP (Matsumoto, col. 3, lines 11-22). In view of this disclosure, it appears that Matsumoto uses "external" to describe a device off-chip within the same system as the DSP as opposed to on the same chip as the DSP. There is no disclosure or suggestion that the referenced "external device or system" is different than the "external memory." Further, the "external device or system" is described in conjunction with data communication between the DSP and the data RAM, which, as noted above, is off-chip but not

included in a system external to the DSP. As Matsumoto merely discloses different techniques for a DSP to communicate with a memory or other device connected to the DSP via a data bus, nothing in Matsumoto suggests that the use of "external" to describe "device or system" has a different meaning than when used to describe the "data memory." (Matsumoto, FIG. 1; col. 4, lines 1-2).

In particular, Matsumoto discloses that the musical tone signal processing device includes an "external data memory, i.e., a data random-access memory (RAM)" which is within the musical tone signal processing device but is external to the DSP. As disclosed in Matsumoto, an "external data memory," depicted by data RAM 14 in Figure 1, communicates with a DSP (Matsumoto, col. 3, lines 11-22). Hence, the use of "external" refers to a memory not on the same chip as the DSP but within the same system as the DSP, processor and memory (Matsumoto, col. 2, lines 2-10). Thus, the "external data memory" disclosed in Matsumoto, like the disclosed processor and memory is only off-chip memory rather than external to the system that includes the DSP. Hence, Matsumoto, like Kawai, merely discloses an off-chip device that is within the same system as the DSP rather than "a system external to the computer," as claimed.

Further, Matsumoto also fails to disclose a register or other storage device which "stores a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer." The data in Matsumoto merely specifies whether to read or write data from memory and does not disclose storing information associated with the completion of a data transfer (Matsumoto, col. 7, lines 56-67). Hence, Matsumoto fails to disclose storing "a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer," as claimed.

In the Final Office Action dated September 18, 2007, the Examiner asserts that "once DSP-2 is finished sending data to the external memory, it sends a status signal to the DMA controller of DSP-1 informing DSP-1 that is it now ready to receive data." *See* Final Office Action dated September 18, 2007, ¶ 4, page 4. Transferring data between DSP-1 and DSP-2 does not constitute transferring a data unit "to a system external to the computer," as claimed. As disclosed in Kawai, DSP-1 and DSP-2, are both included in the same multi-processor system. *See* Kawai, FIG. 5, col. 7, lines 1-10. Hence, the status signal cited by the Examiner merely indicates whether different DSPs are transmitting or receiving data. *See* Kawai, col. 9, lines 12-25. As Kawai only describes communication between DSPs within a single system, there is no disclosure or suggestion of generating a status signal after transferring data to an external system, as claimed.

By failing to provide any references that disclose or suggest "a register that stores a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer," "means for storing a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer system," or "a memory configured to store status data generated by an Input/Output (I/O) device after a data unit transfer between the computer system memory and a system external to the computer system," the Examiner has failed to establish *prima facie* obviousness. Therefore, it is respectfully requested that the final rejections of independent claims 21, 26 and 30 be withdrawn.

Independent claim 34 recites a data transmission method comprising:

> transferring a data unit between a memory in a computer system and a system external to the computer system using a memory access controller coupled to a memory and an Input/Output (I/O) device;
>
> generating status data using the I/O device, the status data indicating completion of the data unit transfer; and

storing the status data in the memory.

Similar to claims 21, 26 and 30, claim 34 recites storing status data after completing a data unit transfer to a system external to the computer system, so the above discussion regarding the deficiencies of Kawai and Matsumoto is hereby incorporated so as to apply to claim 34.

By failing to provide any references that disclose or suggest "transferring a data unit between a memory in a computer system and a system external to the computer system using a memory access controller coupled to a memory and an Input/Output (I/O) device," or "generating status data using the I/O device, the status data indicating completion of the data unit transfer" and "storing the status data in the memory," as recited in claim 34, the Examiner has failed to establish a *prima facie* case of obviousness; therefore it is respectfully requested that the final rejection of independent claim 34 be withdrawn.

As dependent claims 22-25, 27-29, 31-33, 35 and 36 include the limitations of their respective base claims, the rejections of these claims are also improper.

Conclusion

For the foregoing reasons, the Examiner's rejection of claims 21-36 was erroneous, and reversal of his decision is respectfully requested.

Respectfully submitted,
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Appendix: Claims Involved in Appeal

21. A memory access controller adapted to be coupled to a computer system memory and an Input/Output (I/O) device, comprising:

a register that stores a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer; and

circuitry coupled to the register that receives the data status signal and for controlling subsequent operation of the memory access controller based on the data status signal.

22. The controller of claim 21 wherein the data status signal indicates an end of the data unit.

23. The controller of claim 21 wherein the memory access controller executes an instruction in response to the data status signal.

24. The controller of claim 21 wherein the data status signal is used to prompt the memory access controller to request information from the I/O device.

25. The controller of claim 21 wherein the data status signal is used to keep a channel process active.

26. A memory access controller adapted to be coupled to a computer system memory and an Input/Output (I/O) device, comprising:

means for storing a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer system; and

means for controlling subsequent operation of the memory access controller using the data status signal.

27. The memory access controller of claim 26, wherein the data status signal indicates an end of the data unit.

28. The memory access controller of claim 26, wherein the memory access controller further comprises:

means for executing an instruction in response to the data status signal.

29. The memory access controller of claim 26, wherein the data status signal is used to prompt the memory access controller to request information from the I/O device.

30. A memory access controller adapted to be coupled to a memory of a computer system, comprising:

a memory configured to store status data generated by an Input/Output (I/O) device after a data unit transfer between the computer system memory and a system external to the computer system; and

a circuit capable of using the status data.

31. The memory access controller of claim 30, where the I/O device generates the status data after a data unit transfer from the computer system memory to the system external to the computer system.

32. The memory access controller of claim 30, wherein the circuit is capable of using the status data to control any subsequent data unit transfers between the computer system memory and the system external to the computer system.

33. The memory access controller of claim 30, wherein the memory is configured to store status data is a register and the computer system is a computer.

34. A data transmission method, comprising:

transferring a data unit between a memory in a computer system and a system external to the computer system using a memory access controller coupled to a memory and an Input/Output (I/O) device;

generating status data using the I/O device, the status data indicating completion of the data unit transfer;

storing the status data in the memory; and

using the status data to control subsequent operation of the memory access controller.

35. The data transmission method of claim 34, wherein the status data indicate completion of a data unit transfer from the memory in the computer system to the system external to the computer system.

36. The data transmission method of claim 34, further comprising:

determining whether the status data in the memory indicate completion of the data unit transfer; and

transferring another data unit between the memory in the computer system and the system external to the computer system after determining that the data in the memory indicate completion of the data transfer.

Evidence Appendix

None.

Related Proceedings Appendix

None.